A-DATA announces the Number-1 DDR2-800 module which is the first one to achieve the 800MHz of DDR2 speed in the world and pass the ATI Radeon Xpress200 QVL, and this amazing module is available now. This module configuration is by 64M x 8 (512Mbit) die, 8 pcs dies in 1 rank. DDR2-800 is officially supported by AMD AM2 and Intel x965 Platforms.

This Vitesta DDR2 module is designed to meet the 800MHz data-rate specification of the JEDEC (Joint Electron Device Engineering Council) standard, but it seems to own the huge potentiality to draw out higher performance in A-DATA laboratories.

By 1.8V low-voltage application, DDR2 modules can reduce about 50% power consumption, which is compared with 2.5V (DDR) power supply on the same operation speed. So it is an environment-friendly product. In order to achieve so amazing high operation speed, A-DATA applies the lower parasitic-loading FBGA (Fine-pitch BGA) package to run in full-speed without extraneous loading.

Compared with DDR, DDR2 owns four key technologies pave the way to high-speed operation and low power consumption.

4-bit prefetch
DDR2 achieves the high-speed by four times the transmission amount of data. It also doubles the data rate of DDR. In the 4-bit prefetch architecture, READ or WRITE can achieve the four times the amount of data in a really internal bus clock. This is why the DDR2 can operate in four times faster than the internal operation frequency.

ODT (On Die Termination)
In DDR2, it is composed the termination resistor inside which is applied to match the transmission impedance on the mainboard. It will greatly attenuate the reflected noise resulted from last signals which improves a clear logic-level to avoid the reception of error data.

OCD (Off Chip Driver) Calibration
OCD is the Input/Output driver resistance which applied to adjust the cross-voltage to equalize the pull-up and pull-down signal. It will greatly help to the noise-rejected quality from DDR2 module to chipset in mainboard.

Posted CAS & Additive Latency (AL)
In a posted CAS (Column Address Strobe) operation, a CAS signal (READ/WRITE command) can be input to the next clock after RAS (Row Address Strobe) signal (active command) input. The CAS command is held by the module side and executed after the additive latency (0, 1, 2, 3 and 4). It is easier controller design by avoiding collision on the command bus, and improves the command and data bus efficiency due to simple command order. It also improves the practical memory bandwidth by removing the bubble.